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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/810,094
Filing Date: March 26, 2004
Appellant(s): MATSON ET AL.

Michael Rocco Cannatti
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 2/29/2008 appealing from the Office action mailed 6/6/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,473,607	Shohara et al.	10-2002
2003/0028677	Fukuhara	2-2003

6,622,251	Lindskog et al.	9-2003
2002/0059434	Karaoguz et al.	5-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 11-18 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 11-18 are drawn to a "program" per se as recited in the preamble and as such is non-statutory subject matter. See MPEP 2106.IV.B.1.a. Data structures not claimed as embodied in computer readable media are descriptive material per se and are not statutory because they are not capable of causing functional change in the computer. See, e.g., Warmerdam, 33 F.3d at 1361, 31 USPQ2d at 1760 (claim to a data structure per se held nonstatutory). Such claimed data structures do not define any structural and functional interrelationships between the data structure and other claim aspects of the invention, which permit the data structure's functionality to be realized. In contrast, a claimed computer readable medium encoded with a data structure defines structural and functional interrelationships between the data structure and the computer software and hardware components which permit the data structure's functionality to be realized, and is thus statutory. Similarly, computer programs claimed as computer listings per se, i.e., the descriptions or expressions of the programs are not

physical "things." They are neither computer components nor statutory processes, as they are not "acts" being performed. Such claimed computer programs do not define any structural and functional interrelationships between the computer program and other claimed elements of a computer, which permit the computer program's functionality to be realized. Note, "computer readable medium encoded with a computer program" would make the claim statutory.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 4-6, 10-11, and 13-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Shohara et al. (US Pat# 6,473,607).

Regarding claim 1, Shohara's communication device with a self-calibrating sleep timer teaches a processing unit 42 or 50 (Fig. 1); an instruction pipeline circuit (Col. 5 lines 21-32); at least one processing module 42 or 50 (Fig. 1); a timer for generating a time-out interval 70 (Fig. 1); and power control logic 42 or 60 (Fig. 2) for detecting a sleep instruction and placing the processing unit, instruction pipeline circuit and at least one processing module in a low-power state (Col. 10 lines 39-41 and Col. 12 lines 52-64), where the power control logic is operative in response to a wake-up signal (Col. 6 line 59-Col. 7 line 32) to reactivate the instruction pipeline circuit, and consequently at

least one processing module only to the extent required by the wake-up signal (Col. 12 lines 32-64, Col. 13 lines 11-13, and Col. 13 lines 61-65).

Regarding claim 2, Shohara teaches where the instruction pipeline circuit comprises a multi-stage instruction pipeline circuit (Col. 5 lines 21-32).

Regarding claim 4, Shohara teaches where the power control logic comprises instruction decode logic to detect the sleep instruction (Col. 6 line 59-Col. 7 line 32).

Regarding claim 5, Shohara teaches where the power control logic comprises branch condition logic to respond to the wake-up signal (Col. 6 line 59-Col. 7 line 32).

Regarding claim 6, Shohara teaches where the power control logic, having specified one or more wake-up conditions that the processing unit will respond to when in a low-power state, generates the wake-up signal upon detecting the one or more wake-up conditions or the time-out interval (Col. 6 line 59-Col. 7 line 32 and Col. 12 lines 32-64).

Regarding claim 8, Shohara teaches where the power control logic instructs the instruction pipeline circuit to cease fetching new instructions after encountering a sleep instruction whose wake-up conditions are currently deasserted (Col. 5 lines 21-64,Col. 10 lines 39-41, Col. 12 lines 52-64, and Col. 14 line 65-Col. 15 line 7).

Regarding claim 10, Shohara teaches wherein the wake-up conditions and time-out interval are stored in a register by the power control logic (Col. 6 line 59-60 and Col. 5 lines 21-26).

Regarding claim 11, recordable medium claim is rejected for the same reason as apparatus claim 1 since the recited elements would perform the claimed steps.

Regarding claim 13, Shohara teaches wherein the instruction pipeline comprises a multistage instruction pipeline, and the processing device reactivates only stages in the multistage instruction pipeline and/or the function units needed to process one or more instructions necessary to analyze and respond to the wake-up signal (Col. 5 lines 21-32).

Regarding claim 14, Shohara teaches a register for holding the specified wake-up conditions and time out signal.

Regarding claim 16, Shohara teaches where the executable instructions and data comprise control logic 60 (Fig. 2) for controlling the operation of the processing device (Col. 15 lines 37-39).

Regarding claim 17, Shohara teaches where the processing device powers down the one or more processor modules by freezing a clock signal for said one or more modules (Col. 12 lines 52-56).

Regarding claim 18, Shohara teaches where the processing device powers down the one or more processor modules by placing said one or more modules in an idle mode (Col. 12 lines 52-56).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shohara et al. (US Pat# 6,473,607) in view of Fukuhara (US Pat Pub# 2003/0028677).

Regarding claim 3, Shohara's communication device with a self-calibrating sleep timer teaches the limitations in claim 1. Shohara fails to teach a logical OR.

Fukuhara's network device teaches where the wake-up signal comprises a logical OR combination (Section 0016).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate a logical OR as taught by Fukuhara into Shohara's communication device with a self-calibrating sleep timer in order to reduce the consumption of unnecessary electric power (Section 0027).

6. Claims 7, 12, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shohara et al. (US Pat# 6,473,607) in view of Lindskog et al. (US Pat# 6,622,251).

Regarding claim 7, Shohara's communication device with a self-calibrating sleep timer teaches the limitations in claim 1. Shohara fails to teach completing any instructions before sleep mode.

Lindskog's mobile terminal teaches where the power control logic instructs the instruction pipeline circuit to complete any instructions preceding the sleep instruction (Col. 2 lines 48-65 and Col. 4 lines 44-55).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate completing any instructions before sleep mode as taught by Lindskog into Shohara's communication

device with a self-calibrating sleep timer in order to improve on power saving techniques (Col. 5 lines 4-17).

Regarding claim 12, the combination including Lindskog teaches wherein the processing device executes any instructions received by the instruction pipeline before the sleep instruction is received (Col. 2 lines 48-65 and Col. 4 lines 44-55).

Regarding claim 19, Shohara teaches storing one or more wake-up conditions and a time-out interval in a register 24 (Fig. 1, Col. 6 line 59-60, and Col. 5 lines 21-26); receiving a processor sleep instruction (Col. 5 lines 21-33, Col. 6 line 59- Col. 7 line 32, Col. 10 lines 39-41, and Col. 12 lines 52-64); executing any pending instructions received by the processor before the sleep instruction (Col. 5 lines 21-64); powering down the one or more processor modules (Col. 5 lines 21-33, Col. 6 line 59-Col. 7 line 32, Col. 10 lines 39-41, and Col. 12 lines 52-64); receiving a processor wake-up signal corresponding to one of said wake-up conditions or said time-out interval (Col. 6 line 59-Col. 7 line 32); powering up only the processor modules required to respond to the detected processor wake-up signal (Col. 6 line 59-Col. 7 line 32, Col. 12 lines 32-64, Col. 13 lines 11-13, and Col. 13 lines 61-65). Shohara fails to teach executing any pending instructions received by the processor before the sleep instruction.

Lindskog teaches executing any pending instructions received by the processor before the sleep instruction (Col. 2 lines 48-65 and Col. 4 lines 44-55).

Regarding claim 20, the combination including Shohara teaches wherein one of the processor modules comprises an instruction pipeline circuit (Col. 5 lines 21-32).

7. Claims 9 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shohara et al. (US Pat# 6,473,607) in view of Karaoguz et al. (US Pat Pub# 2002/0059434).

Regarding claim 9, Shohara's communication device with a self-calibrating sleep timer teaches the limitations in claim 1. Shohara fails to teach using CMOS processing.

Karaoguz's communication device teaches a circuit and at least one processing module are formed together on a common silicon substrate using CMOS processing (Section 0071).

Therefore, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time the invention was made to incorporate using CMOS processing as taught by Karaoguz into Shohara's communication device with a self-calibrating sleep timer in order to communicate with a variety of networks (Section 0008).

Regarding claim 15, the combination including Karaoguz teaches where the processing device is implemented as part of a single-chip wireless communication device (Section 0071).

(10) Response to Argument

1. Appellant's arguments with respect to claims 1-20 have been fully considered but they are not persuasive.

(A) The appellant argued that "because this amendment was submitted to comply with a requirement of form set forth in the previous Office Action, Applicants submit that the amendment was permitted under 35 CFR 1.116(b)(1), and therefore

respectfully request that the statutory subject matter rejection of claims 1-18 under 35 U.S.C. 101 be withdrawn and that the amended claims be allowed."

In response to the argument (A), the amendment filed on 9/6/2007 was not entered on advisory action 9/21/2007 because the scope of claim 19 was changed and therefore claim 11 amendment to clean up the claim language can not be entered as of right now. Therefore, the 101 rejection for claim 11 is still rejected.

(B) The appellant argued that Shohara "fails to disclose an 'instruction pipeline circuit,' much less Applicants' scheme for using detected sleep instructions and wakeup signal to selectively power down and reactivate processing modules in the instruction pipeline circuit only to the extent required by the sleep instruction and the wake-up signal."

In response to the argument (B), the examiner respectfully disagrees with the appellant's argument. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., instruction pipeline) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Examiner believes appellant is reading more into the claim than present. The claim only states the limitation of an "instruction pipeline circuit" and does not define the term any further in the claim. Based on the broadest reasonable interpretation of "instruction pipeline" the examiner reads the controller 50 (Figs. 1 and 2) to read on an instruction pipeline because in column 1 lines 21-63 it

teaches the controller carrying out many instructions through a pipeline (lines connected to different components i.e. 26, 28, 42, 34, 24 of figure 1) to components in powering on or off different components (Col. 10 lines 39-41 and Col. 12 lines 52-64).

(C) The appellant submits "'instruction pipeline' refers to a processing structure that separates the execution of instructions into multiple stages (e.g., instruction fetch, instruction decode and operand read, execution, and write), and executes separate instructions in each stage simultaneously, thereby allowing multiple instructions to be executed concurrently."

In response to the argument (C), the examiner respectfully disagrees with the appellant's argument. Again, as in (B), this limitation defining an instruction pipeline is not claimed. However, for the sake of argument in column 5 lines 21-26 and column 11 lines 18-33 of Shohara teaches a controller that is fetching instructions, decoding, reading, executing, and writing (obvious there is memory). In column 12 lines 40-46 of Shohara it teaches the instructions execute simultaneously (data processing and decoding).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Andrew Wendell/

Examiner, Art Unit 2618

March 24, 2008

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